WHAT IS CLAIMED IS:

1. A parallel sense amplifier including a measuring branch for receiving an input current to be measured, a plurality of reference branches each one for receiving a reference current, and a plurality of comparators each one for comparing a voltage at a measuring node along the measuring branch with a voltage at a reference node along a corresponding reference branch,

wherein the amplifier further includes a multiple current mirror for mirroring the input current into each reference branch.

2. The amplifier according to claim 1, wherein the current mirror has a mirroring factor being substantially equal to 1.

3. The amplifier according to claim 1, wherein the current mirror includes an input branch having an input transistor being diode-connected and a plurality of output branches each one having a corresponding output transistor, the input branch being included in the measuring branch and each output branch being included in a corresponding reference branch.

4. The amplifier according to claim 3, wherein each comparator has a first input terminal and a second input terminal, and wherein each transistor has a first terminal, a second terminal and a control terminal, the first terminal of all the transistors being connected to a power supply terminal, the second terminal of the input transistor defining the measuring node being connected to the first input terminal of each comparator and the second terminal of each output transistor defining the corresponding reference node being connected to the second input terminal of the corresponding comparator, and the control terminal of the input transistor being connected to the second terminal of the input transistor and to the control terminals of all the output transistors.

5. The amplifier according to claim 4, wherein the transistors have substantially equal sizes.

6. The amplifier according to claim 1, further including a plurality of pre-charging blocks each one for pre-charging a corresponding branch of the sense amplifier in response to a first enabling signal having a first length, a plurality of equalizing blocks each one for equalizing the measuring branch with a

corresponding reference branch in response to a second enabling signal having a second length longer than the first length, and means for generating the first and the second enabling signals.

7. The amplifier according to claim 6, wherein the means for generating the first and the second enabling signals includes first delaying means for generating the first enabling signal in response to a triggering signal of a sensing operation and second delaying means for generating the second enabling signal in response to the first enabling signal.

8. A non-volatile multilevel memory device including a plurality of memory cells each one being programmable to more than two levels, means for selecting at least one memory cell to be read, and at least one parallel sense amplifier according to claim 1 each one for reading a corresponding selected memory cell.

9. The memory device according to claim 8, wherein the memory device is of the asynchronous type and includes means for receiving an address for selecting the memory cells and means for generating a detection pulse in response to an address transition, the first delaying means generating the first enabling signal in response to the detection pulse.

10. A method of operating a parallel sense amplifier including the steps of:

providing an input current to be measured to a measuring branch,

providing each one of a plurality of reference currents to a corresponding reference branch,

comparing a voltage at a measuring node along the measuring branch with a voltage at a reference node along each reference branch, and

mirroring the input current into each reference branch.

11. A sense amplifier, comprising:

an input branch operable to conduct an input current having an amplitude and to generate an input signal that is related to the input current;

a first output branch coupled to the input branch and operable to generate a first output signal that is related to a combination of a first reference current and a first mirror current that is related to the input current; and

a comparator circuit coupled to the input and first output branches and operable to determine the amplitude of the input current from the input signal and the first output signal.

12. The sense amplifier of claim 11 wherein:
the input signal comprises an input voltage; and
the first output signal comprises a first output voltage.

13. The sense amplifier of claim 11 wherein the first output signal is related to a difference between the first reference current and the first mirror current.

14. The sense amplifier of claim 11 wherein the first output signal is related to a ratio between the first reference current and the first mirror current.

15. The sense amplifier of claim 11 wherein the first output branch is operable to conduct the smaller of the first reference current and the first mirror current.

16. The sense amplifier of claim 11 wherein the first mirror current is proportional to the input current.

17. The sense amplifier of claim 11 wherein the first mirror current is substantially equal to the input current.

18. The sense amplifier of claim 11 wherein the comparator circuit comprises a first comparator having first and second input nodes and an output node and that is operable to:
receive the input and first output signals on the first and second input nodes, respectively;
generate on the output node a comparison signal having a first state if the input signal is greater than the first output signal; and
generate the comparison signal having a second state if the input signal is less than the first output signal.

19. The sense amplifier of claim 11, further comprising:
a second output branch coupled to the input branch and operable to generate a second output signal that is related to a combination of a second

reference current and a second mirror current that is related to the input current; and

wherein the comparator circuit is coupled to the second output branch and is operable to determine the amplitude of the input current from the second output signal.

20. The sense amplifier of claim 11, further comprising:

a second output branch coupled to the input branch and operable to generate a second output signal that is related to a combination of a second reference current and a second mirror current that is related to the input current;

a third output branch coupled to the input branch and operable to generate a third output signal that is related to a combination of a third reference current and a third mirror current that is related to the input current; and

wherein the comparator circuit is coupled to the second and third output branches and is operable to determine the amplitude of the input current from the second and third output signals.

21. The sense amplifier of claim 11, further comprising:

a second output branch coupled to the input branch and operable to generate a second output signal that is related to a combination of a second reference current and a second mirror current that is related to the input current;

a third output branch coupled to the input branch and operable to generate a third output signal that is related to a combination of a third reference current and a third mirror current that is related to the input current; and

wherein the comparator circuit is coupled to the second and third output branches and comprises,

a first comparator that is operable to receive the input and first output signals and to generate a comparison signal having a first state if the input signal is greater than the first output signal and having a second state if the input signal is less than the first output signal,

a second comparator that is operable to receive the input and second output signals and to generate a second comparison signal having a third state if the input signal is greater than the second output signal and having a fourth state if the input signal is less than the second output signal,

a third comparator that is operable to receive the input and third output signals and to generate a third comparison signal having a fifth state if the input signal is greater than the third output signal and having a sixth state if the input signal is less than the third output signal; and

an encoder operable to generate from the first, second, and third comparison signals a digital value that represents the amplitude of the input signal.

22. A memory circuit, comprising:

a memory cell operable to generate a read current during a read cycle, the read current representing a data value stored in the memory cell;

a reference cell operable to generate a reference current during the read cycle; and

sense amplifier operable to be coupled to the memory cell and to the reference cell during the read cycle, the sense amplifier comprising,

an input branch operable to conduct the read current and to generate an input signal that is related to the read current,

an output branch coupled to the input branch and operable to generate an output signal that is related to a combination of the reference current and a mirror current that is related to the read current, and

a comparator circuit coupled to the input and output branches and operable to determine the data value from the input and output signals.

23. An electronic system, comprising:

a processor;

a memory circuit coupled to the processor and including,

a memory cell operable to generate a read current during a read cycle, the read current representing a data value stored in the memory cell,

a reference cell operable to generate a reference current during the read cycle, and

sense amplifier operable to be coupled to the memory cell and to the reference cell during the read cycle, the sense amplifier comprising,

an input branch operable to conduct the read current and to generate an input signal that is related to the read current,

an output branch coupled to the input branch and operable to generate an output signal that is related to a combination of the reference current and a mirror current that is related to the read current, and

a comparator circuit coupled to the input and output branches and operable to determine the data value from the input and output signals.

24. A sense amplifier, comprising:

a supply terminal;

a first transistor having a first node coupled to the supply terminal, a second node operable to receive an input current, and a control node coupled to the second node;

a second transistor having a first node coupled to the supply terminal, a second node operable to be coupled to a first reference-current generator, and a control node coupled to the control node of the first transistor; and

a first comparator having a first input node coupled to the second node of the second transistor and having a second input node coupled to the control node of the first transistor.

25. The sense amplifier of claim 24 wherein:

the first and second transistors comprise respective PMOS transistors; and

wherein the first and second input nodes of the comparator respectively comprise non-inverting and inverting nodes.

26. The sense amplifier of claim 24, further comprising:

a third transistor having a first node coupled to the supply terminal, a second node operable to be coupled to a second reference-current generator, and a control node coupled to the control node of the first transistor;

wherein the first comparator has an output node;

a second comparator having a first input node coupled to the second node of the third transistor, a second input node coupled to the control node of the first transistor, and an output node; and

an encoder coupled to the output nodes of the first and second comparators and operable to generate a digital value that represents the input current.

27. A method, comprising:

generating an input signal in response to an input current;

generating a first output signal in response to a combination of a first reference current and a first output current that is related to the input current; and

determining a value of the input current from the input signal and the first output signal.

28. The method of claim 27, further comprising:

generating the input current with a memory cell during a read cycle; and

generating the first reference current with a reference cell during the read cycle.

29. The method of claim 27 wherein generating the first output signal comprises:

conducting the smaller of the first reference current and the first output current through a conductive path; and

generating the first output signal at a node of the conductive path.

30. The method of claim 27, further comprising:

generating a second output signal in response to a combination of a second reference current and a second output current that is related to the input current; and

wherein determining the value of the input current comprises determining the value of the input current from the input signal and the first and second output signals.